Analysis Of Harmonic Mitigation Techniques For Cascaded Asymmetric Inverters

Lakshmi PRASANNA[1], *Jyothsna.T.R.*[2]

[1]Electrical Engineering, Research Scholar, Andhra University, Maddilapalem, Visakhapatnam, India
[2]Electrical Engineering, Professor, Andhra University, Maddilapalem, Visakhapatnam, India

lakshmiprasanna.rs@andhrauniversity.edu.in, Thummalajyothsna@gmail.com

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Abstract. *Multilevel inverters (MLIs) are attracting the attention of academics as well as industry as a feasible technology for an extensive variety of purposes, like renewable energy sources, and Electric vehicles. MLIs are commonly employed as a part of the sophisticated converter configurations in both high and medium voltage applications. The creation of minimised switch MLI structures remains a key objective of the present research with the goal to achieve superior results despite of involved a greater number of switches. Basically, various layouts of asymmetrical configuration using enhanced cascaded bridge topologies are identified in a brief overview and evaluated against important parameters. It is a method of designing multiple voltage levels using identical switch count and fewer devices. This work describes numerous varieties of harmonic mitigation techniques, and it also outlines the most effective switching angle optimizations to produce various levels. Furthermore, the effectiveness of configuration is evaluated based on minimising THD due to decreasing lower order harmonics. THD is evaluated against various mitigation techniques employing certain proportions of source voltages coming from solar energy /batteries. THD is calculated theoretically and contrasted to simulation outcomes for the suggested configurations. The simulated waveforms of various configurations are examined using Hardware in loop (HIL) application.*

Keywords

Asymmetric Inverter, Harmonic mitigation techniques, Low frequency scheme, Total Harmonic Distortion,OPAL-RT(OP4510).

1. Introduction

The incorporation of renewable energy sources into the currently operating power network significantly improved system reliability. The most important environmentally friendly power sources are solar and wind energies. Solar energy interconnection necessitates the inclusion of converters, a type of simply dc to ac converters. The primary features of implementing MLIs in applications such as electric vehicles and renewable energy sources are enhanced power density, greater effectiveness, less harmonic distortion, more effective voltage control, flexibility, adaptability, and compatibility with renewable energy sources. MLIs are a desirable option for a variety of applications in the renewable energy and electric vehicle sectors due to these advantages MLIs are frequently utilised for such applications [1, 2].

Classic MLI configurations such as neutral point clamped MLI (NPCMLI), cascaded H-bridge MLI (CHBMLI), and flying capacitor MLI (FCMLI) have become commonplace in practical applications. The CHB inverter topology necessitate minimal component count than other conventional inverter topologies for creating an identical level of output. CHB inverters are transitioning from a traditional perspective to real-world applications due to capabilities that includes high degree of modularity, the ability to safely link to medium voltage with superior power quality [3, 4].

As a result, MLIs using fewer components are employed in recent studies to create the identical number of levels identical to the traditional configuration. Despite this, the approach of minimizing component counts displays certain difficulties to academics. However, researchers encountered a few obstacles while

attempting to minimize component counts, such as enhanced rated voltage of switching devices, losses in extensibility, minimization of concurrent modes count, occasionally demand of bidirectional switches, advanced control methodologies, a massive number of sources to accomplish the anticipated level count from the existing topologies [5–9]. Nevertheless, by integrating sustainable energy sources to act as independent input for the cascade inverters, this drawback can be rectified. In comparison to other conventional inverter structures, the CHBMLI needs less switch count and all other factors taking into count to create identical voltage levels in the output [10].

By utilising improved cascaded bridge topologies in asymmetrical configurations, it is possible to achieve multiple voltage levels with a minimum number of switches by considering benefits of asymmetric voltage division. These configurations are desirable for a wide range of applications since they offer positive aspects like less switch count, optimized number of levels, greater efficiency, and improved fault tolerance. Due to features such as a good extent of modularity, the ability to securely connect to medium voltage, and good power quality CHB inverters transitioned from a traditional view to real world applications. Subject to the level of output voltage CHBMLI is generally called symmetric or asymmetric. Those are (i) equal voltage cascaded MLI(ECHBMLI), where all input voltages are in equal magnitude, (ii)natural sequence cascaded MLI(NSCHBMLI), where all input voltage follows arithmetic progression each is differed by one, (iii) binary cascaded MLI(BCHBMLI), where successive input voltages are doubled,(iv)trinary cascaded MLI(TCHBMLI), in which successive input voltages are tripled,(v)quasi-linear cascade MLI(QLCHBMLI), where all input voltages are kept constant so that the anticipated resulting voltage is reached.

Modulation techniques are the fundamental aspects for any MLI structure. In fact, suggesting novel modulation schemes that can be implemented for any type of structure in order to meet specified requirements can be viewed as a distinct area of research [9,13]. Modulation is the process of control the voltage waveform using switches to meet specified requirements. MLI modulation schemes are commonly categorized as high frequency (HF) or low frequency (LF). In [27], fifteen level configuration is described utilizing high frequency control scheme. Hybrid modulation scheme is employed for fifteen level topology described in [26]. The low frequency control scheme possesses numerous significant features, which includes (a) highly efficient with low frequency to fundamental frequency proportion; (b) excellent voltage boosting and a wide converter capacity; (c) fewer filter demands; (d) complete omission of lower harmonics; (e) low switching losses with restricted harmonic regulation; and (f) additionally performance index is optimised for various superior aspects. Various modulation schemes for 15-level topology are presented [23, 24]. The worth of utilizing a LF scheme than HF scheme are reduced switching losses, minimum stress on switches, improved device utilization factor, and enhanced converter efficiency. Selective harmonic elimination (SHE), nearest level control (NLC), and space vector control (SVC) are some of the popular LF schemes [11,12]. Utilizing NLC fifteen level is developed in [25]. Employing NLC distinct thirteen level topologies designed [28–30]. If greater the number of levels, SVC is a reasonable technique only issue is it does not eliminate specific harmonic. The above problem is mitigated using the SHE method by adjusting the switch angles mentioned in [10,14]. Review of SHE technique algorithms described [18–20]. Minimization of harmonics utilizing Particle Swarm Optimization (PSO) approach for symmetrical MLI configuration is presented [15, 17]. Furthermore, PSO approach [21] is lacking to estimate switching angles for specified modulation indices (ma) based on computational results from Genetic Algorithm (GA) approach [22]. As the level of output extents, obtain solutions using SHE become more challenging to implement. As a consequence, another straightforward approach of SHE addresses above issue have been executed in [16], that is harmonic mitigation which involves remarkable minimization of lower order harmonics rather than entirely eradicating them.

An asymmetrical cascaded bridge MLI topology is proposed in this work, as well as mitigation techniques. The following positive aspects are offered by the recommended work:

- The application to mitigation techniques has been efficiently carried out, it is easily resolved to configure up mathematical analysis and leads to lower voltage stress.
- It operates efficiently with a wide range of loads.
- The article outlines an open-loop structure and new cascade asymmetric inverters that are tested using the OPAL-RT simulator.

This work has the following structure Section 2. confronts proposed topologies with all switching states for thirteen and fifteen respectively. Section 3. focuses on mitigation techniques, Voltage stress analysis and Loss analysis. Section 4. explores simulation results, Thermal modelling and HIL Implementation, Section 5. compares proposed asymmetrical configurations with other topologies and Section 6. refers to conclusion of work.

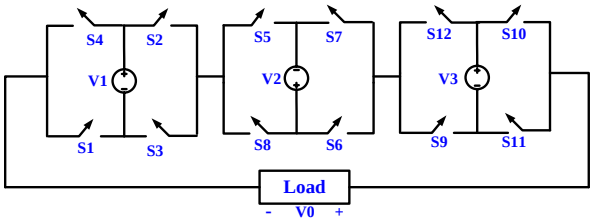


Fig. 1: Proposed Topology

2. Proposed Topology

Figure 1 shows the planned H-bridge configuration before learning more about configurations. It has three voltage sources and twelve switches that are IGBTs in antiparallel with diodes. The following subsections detail the switching states and modes of operation for the voltage sources that are classed as 13-level, and 15-level configurations based on ratings.

2.1. Thirteen-Level Configuration

Figure 2 shows the switching states for this method, which is a part of the NSCHBMLI. In Figure 2, red denotes the conducting path of the matching switches, while green denotes the non-conducting path. Twelve switches are in view with three preferred voltage sources are arranged as a natural sequence magnitudes while creating levels. Since voltage sources are rated the same, all switches are also rated the same. table 1 represents the switching capabilities of switches for creating the required level of voltage. Table 1 displays 0 for no conductivity and 1 for conductivity of the switches. The remaining switches, such as S_4, S_3, S_8, S_7, S_{12}, and S_{11} illustrated in figure 2, are complementary operations of the switches as indicated above and are shown in table1 as S_1, S_2, S_5, S_6, S_9, and S_{10}. The operating mode of this configuration is based on NSCHBMLI therefore, the peak output is expressed as equation (1). The following details the configuration's operating mode:

$$V_{opeak} = \sum_{n=1}^{\infty} \left(\frac{n(n+1)}{2} \right) V_{dc}. \qquad (1)$$

$0V_{dc}$: To achieve zero output voltage level in this mode of operation, either S_1, S_3, S_6, S_8, S_9, and S_{11} conduct or S_2, S_4, S_5, S_7, S_{10}, and S_{12} conduct, as shown in Figure 2(d)&2(f) and Table 1(7) mode, respectively.

$\pm 1V_{dc}$: S_1, S_2, S_6, S_8, S_9, and S_{11} conduct in accordance with the indications in Figure 2(c) and Table 1(6) mode to obtain $+1V_{dc}$ as the output voltage level. To obtain $-1V_{dc}$ as the output voltage level, S_3, S_4, S_5, S_7, S_{10}, and S_{12} conduct as shown in Figure 2(f) and Table 1(8) mode respectively.

$\pm 2V_{dc}$: S_1, S_3, S_5, S_6, S_9, and S_{11} conduct as shown in Figure 2(b) and Table 1(5) mode to reach $+2V_{dc}$ as the output voltage level. To obtain $-2V_{dc}$ as the output voltage level, S_2, S_4, S_7, S_8, S_{10}, and S_{12} conduct as shown in Figure 2(f) and Table 1(9) mode respectively.

$\pm 3V_{dc}$: S_1, S_3, S_6, S_7, S_9, and S_{10} conduct as shown in Figure 2(c) and Table 1(4) mode, in order to produce $+3V_{dc}$ as the output voltage level. S_2, S_4, S_5, S_7, S_{11}, and S_{12} conduct in the order depicted in Figure 2(j) and Table 1(10) mode respectively, to produce an output voltage level of $-3V_{dc}$.

$\pm 4V_{dc}$: As illustrated in Figure 2(b) and Table 1(3) mode, the switching pattern for producing $+4V_{dc}$ as the output voltage level. The conductivity pattern of the switches is depicted in Figure 2(k) and Table 1(11) mode respectively to obtain $-4V_{dc}$ as the output voltage level.

$\pm 5V_{dc}$: Figure 2(a) and Table 1(2) mode, which demonstrate the switching patterns used to provide $+5V_{dc}$ as the output voltage level, respectively. As illustrated in Figure 2(l) and Table 1(12) mode, the switching pattern used to generate $-5V_{dc}$ as the output voltage level.

$\pm 6V_{dc}$: S_1, S_2, S_5, S_6, S_9, and S_{10} conduct in the manner depicted in Figure 2(a) and Table 1(1) mode respectively, to produce an output voltage level of $+6V_{dc}$. S_3, S_4, S_7, S_8, S_{11}, and S_{12} conduct as illustrated in Figure 2(h) and Table 1(13) respectively, to produce an output voltage level of $-6V_{dc}$.

Tab. 1: Operating modes of 13-level configuration

Switching Action						Mode	V_{output}
S_1	S_2	S_5	S_6	S_9	S_{10}		
1	1	1	1	1	1	1	$+6V_{dc}$
1	0	1	1	1	1	2	$+5V_{dc}$
0	0	1	1	1	1	3	$+4V_{dc}$
1	0	0	1	1	1	4	$+3V_{dc}$
1	0	1	1	1	0	5	$+2V_{dc}$
1	1	0	1	1	0	6	$+1V_{dc}$
1	0	0	1	1	0	7	0
0	0	1	0	0	1	8	$-1V_{dc}$
0	1	0	0	0	1	9	$-2V_{dc}$
0	1	1	0	0	0	10	$-3V_{dc}$
1	1	0	0	0	0	11	$-4V_{dc}$
0	1	0	0	0	0	12	$-5V_{dc}$
0	0	0	0	0	0	13	$-6V_{dc}$

2.2. Fifteen-Level Configuration

This design is a variation on the BCHBMLI, and Figures 2&3 illustrates their ways of switching operation. The configuration used in this instance is a binary one with all voltage source ratings. Similar to the example

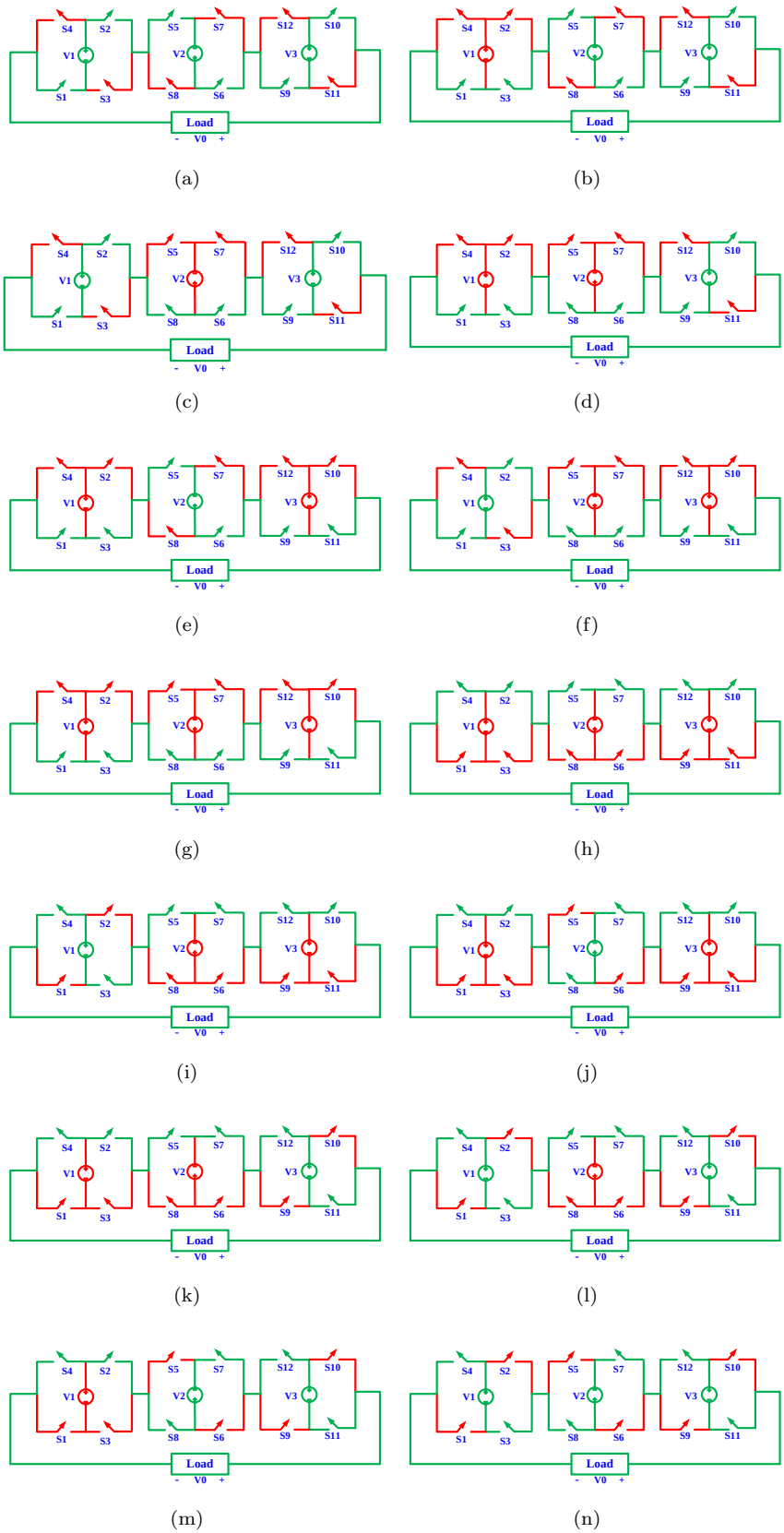


Fig. 2: Operating modes of 13-level configuration with (a) $V_0 = +6V_{dc}$, (b) $V_0 = +5V_{dc}$, (c) $V_0 = +4V_{dc}$, (d) $V_0 = +3V_{dc}$, (e) $V_0 = +2V_{dc}$, (f) $V_0 = +1V_{dc}$, (g) $V_0 = 0$, (h) $V_0 = 0$, (i) $V_0 = -1V_{dc}$, (j) $V_0 = -2V_{dc}$, (k) $V_0 = -3V_{dc}$, (l) $V_0 = -4V_{dc}$, (m) $V_0 = -5V_{dc}$, (n) $V_0 = -6V_{dc}$.

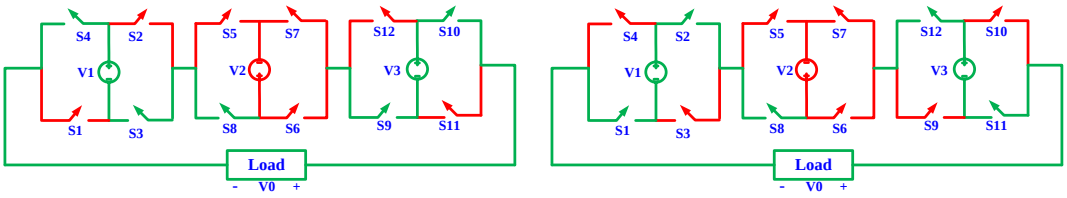


Fig. 3: Two operating modes of 15-level configuration with (a) $V_0 = +3V_{dc}$, (b) $V_0 = -3V_{dc}$.

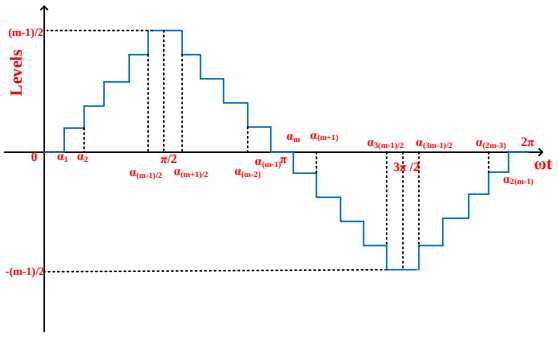


Fig. 4: Multi- level inverter output voltage waveform

given above, the ratings for the first H-bridge switch are different from those for the next two. The switching behaviour for various operating modes is shown in Table 2. The peak output voltage of this configuration is indicated as equation (2). It adheres to the same set of circumstances as described in Table 1. Here is an explanation of how the modes of operation transition.

$$V_{opeak} = \sum_{n=1}^{\infty} (-(1-2^n))V_{dc}. \tag{2}$$

Tab. 2: Switching modes of 15-level configuration

Switching Action						Mode	$\mathbf{V_{output}}$
S_1	S_2	S_5	S_6	S_9	S_{10}		
1	1	1	1	1	1	1	$+7V_{dc}$
1	0	1	1	1	1	2	$+6V_{dc}$
1	1	0	1	1	1	3	$+5V_{dc}$
1	0	0	1	1	1	4	$+4V_{dc}$
1	1	1	1	1	0	5	$+3V_{dc}$
1	0	1	1	1	0	6	$+2V_{dc}$
1	1	0	1	1	0	7	$+1V_{dc}$
1	0	0	1	1	0	8	0
0	0	1	0	0	1	9	$-1V_{dc}$
0	1	0	0	0	1	10	$-2V_{dc}$
0	0	0	0	0	1	11	$-3V_{dc}$
0	1	1	0	0	0	12	$-4V_{dc}$
0	0	1	0	0	0	13	$-5V_{dc}$
0	1	0	0	0	0	14	$-6V_{dc}$
0	0	0	0	0	0	15	$-7V_{dc}$

$0V_{dc}$: As previously mentioned in Table 1(7) mode, the analogous switches are conducted in the same manner for this configuration to achieve zero output voltage level, as demonstrated in Figure 2(g)&2(h) and Table 2(8) mode respectively.

$\pm 1V_{dc}$: As previously mentioned Table 1(6) mode, the path it takes is depicted in Figure 2(f) and Table 2(7) mode respectively, for the creation of $+1V_{dc}$ as the output voltage level. Similar to how Table 1(8) was reproduced in Figure 2(i) and Table 2(9), it is possible to acquire the output voltage level of $-1V_{dc}$.

$\pm 2V_{dc}$: S_1, S_3, S_5, S_6, S_9, and S_{11} conducts are depicted in Figure 2(e) and Table 2(6) mode respectively, for formation of $+2V_{dc}$ as output voltage level. S_2, S_4, S_7, S_8, S_{10}, and S_{12} conducts are illustrated in Figure 2(j) and Table 2(10) mode respectively, for providing $-2V_{dc}$ as output voltage level.

$\pm 3V_{dc}$: In order to provide the $+3V_{dc}$ output voltage level depicted in Figure 3(a) and Table 2(5) mode, S_1, S_2, S_5, S_6, S_9, and S_{11} conduct, respectively. As demonstrated in Figure 3(b) and Table 2(11) mode, respectively, S_3, S_4, S_7, S_8, S_{10}, and S_{12} conduct in the same way to generate the $-3V_{dc}$ output voltage level.

$\pm 4V_{dc}$: In the same way as Table 1(1) mode was described before, Table 2(4) mode and Figure 2(d) both display the $+4V_{dc}$ output voltage level. The output voltage level of $-4V_{dc}$ is produced in the same manner as that described in Table 1(7) mode and is depicted in Figure 2(k) and Table 2(12) mode, respectively.

$\pm 5V_{dc}$: It follows the same conduction path pattern as in Figure 2(c) and produces an output voltage level of $+5V_{dc}$, which is depicted in Table 2(3) mode. Similar to the conduction pattern exhibited in Figure 2(l), it yields $-5V_{dc}$ as the output voltage level depicted in Table 2(13) mode.

$\pm 6V_{dc}$: S_1, S_3, S_5, S_6, S_9, and S_{10} conducts are illustrated in Figure 2(b) and Table 2(2) mode respectively, for formation of $+6V_{dc}$ as output voltage level. S_2, S_4, S_7, S_8, S_{11}, and S_{12} conducts are illustrated in Figure 2(m) and Table 2(14) mode respectively, for providing $-6V_{dc}$ as output voltage level.

$\pm 7V_{dc}$: The same pattern of the switches' conduction path, observed in Figure 2(a), is followed and results in the output voltage level of $+7V_{dc}$, which is represented

in Table 2(1) mode. Following the same conduction path as the switches in Figure 2(n), it produces the output voltage level of $-7V_{dc}$, which is illustrated in Table 2(15) mode.

3. Mitigation Techniques, Voltage Stress Analysis and Loss Analysis

3.1. Mitigation Techniques

The switching angles considered for a quarter wave symmetry is shown in Figure 4. There are 2(m-1) switching angles are expressed in the wave form for an m-level (m is an odd number) output voltage waveform. As seen from Figure 4, switching angles are divided in to four quadrants. The first quadrant (range from 0 to $\pi/2$) switching angles are called as main switching angles. By using main switching angles remaining quadrant angles are calculated easily.

In First quadrant interval (0-$\pi/2$), main switching angles are denoted as

$$\alpha_1, \alpha_2, ..., \alpha_{(m-1)/2}. \tag{3}$$

In second Quadrant interval ($\pi/2-\pi$), the switching angles are represented as

$$\alpha_{(m+1)/2} = \pi - \alpha_{(m-1)/2}, ..., \alpha_{(m-1)} = \pi - \alpha_1. \tag{4}$$

In third quadrant interval($\pi - 3\pi/2$), the switching angles are indicated as

$$\alpha_m = \pi + \alpha_1, ..., \alpha_{3(m-1)/2} = \pi + \alpha_{(m-1)/2}. \tag{5}$$

In fourth quadrant interval($3\pi/2-2\pi$), the switching angles are indicated as

$$\alpha_{(3m-1)/2} = 2\pi - \alpha_{(m-1)/2}, ..., \alpha_{2(m-1)} = 2\pi - \alpha_1. \tag{6}$$

Equal phase method: The formula (7) is capable of being utilized to create an assessment of switching angles in this method. The switching angles are equally distributed, with an average spectrum of 0-$\pi/2$. The number m denotes the generated number of levels.

$$\alpha_i = i * \frac{180}{m}, \tag{7}$$

where $i = 1, 2, \ldots, (m-1)/2$

Half equal phase method: Since the output is too narrow as well as the resulting waveform appears as a triangle in EPM, the HEPM approach has been created to obtain a larger and more effective output from the MLIs. The switching angles in the 0-$\pi/2$ spectrum are calculated using the formula as follows:

$$\alpha_i = i * \frac{180}{(m+1)}. \tag{8}$$

Half Height method: Even though the first two methods can smoothly arrange the main switching angles, the output waveform does not look like a sinusoidal. By using this method, the switching angles in first quadrant are estimated depending on the sine function. The theory is that when sine function value raises to half the altitude of the level, the switching angle is positioned, leading to an improved output wave form. The following formula specifies the main switching angles.

$$\alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right). \tag{9}$$

Tab. 3: Switching angles of thirteen level topology

Method	Main switching angle					
	α_1	α_2	α_3	α_4	α_5	α_6
EPM	13.84	27.69	41.54	55.38	69.23	83.07
HEPM	12.85	25.71	38.57	51.42	64.28	77.14
HHM	4.78	14.47	24.62	35.68	48.59	66.44
FFM	2.39	7.23	12.31	17.84	24.29	33.22

Feed Forward method: Unlike other approaches, this method was designed to minimize the difference between the two half cycles of the output waveform, as shown by the equation (10)

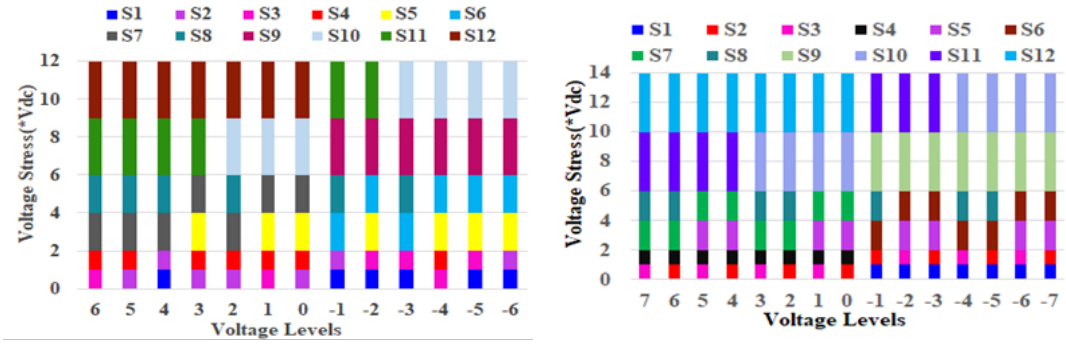
$$\alpha_i = \frac{1}{2}\sin^{-1}\left(\frac{2i-1}{m-1}\right) \tag{10}$$

As a result, the main switching angles are effectively obtained for 'm' number of levels by using four Equations (7)-(10). The calculation of switching angle is independent with respect to other methods as seen from equations (7)-(10). For thirteen level, fifteen level topologies, the main switching angles are calculated based on the four methods and depicted in Table 3&Table 4 respectively.

The formula of Modulation Index (MI) in terms of fundamental maximum voltage (Vm) is expressed as equation (11). From equation (12) it seems that modulation index is modified due to the variation of main switching angles respectively. Therefore, depending on the inverter configuration optimized value of MI changes for various main switching angles respectively.

$$MI = \frac{V_m}{V_1 + V_2 + ... + V_n}, \tag{11}$$

$$V_m = \frac{4}{\pi}\left[V_1\cos\alpha_1 + V_2\cos\alpha_2 + ... + V_n\cos\alpha_{(m-1)/2}\right] \tag{12}$$



(a) (b)

Fig. 5: Voltage stress of switches for distinct configuration with (a) 13-Level, (b) 15-Level.

Tab. 4: Switching angles of fifteen level topology

Method	Main switching angle						
	α_1	α_2	α_3	α_4	α_5	α_6	α_7
EPM	12	24	36	48	60	72	84
HEPM	11.25	22.5	33.75	45	56.25	67.5	78.75
HHM	4.10	12.37	20.92	30.00	40.01	51.79	68.21
FFM	2.05	6.18	10.46	15.00	20.00	25.89	34.10

Tab. 5: Calculated %THD of 13-level and 15-level configurations

Mitigation Method	%THD	
	13-level	15-level
EPM	20.26	18.84
HEPM	18.61	17.54
HHM	6.35	5.5
FFM	21.15	20.67

Theoretical calculation of THD: By using the equation (13) Total Harmonic Distortion (THD) is calculated. Where P is the switching angle count and α is the main switching angle respectively. For example, in case of 13-level inverter P becomes 6 and the first term of numerator changes as $\pi^2 * 36/8$. The remaining two terms is expressed as equation (14) & (15) respectively. Using Table 4 the main switching angles for thirteen level configuration for individual method using equation 14 %THD is calculated. In the same fashion for other suggested configuration, THD formula is expressed. For all the four methods %THD calculated value is expressed in table 5

3.2. Voltage Stress Analysis

Maximum voltage stress of complementary switches has identical magnitudes. The maximum voltage stress of devices is expressed as (16), (17), and (18).

$$V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{dc}, \quad (16)$$

$$V_{s5} = V_{s6} = V_{s7} = V_{s8} = 2V_{dc}, \quad (17)$$

$$V_{s9} = V_{s10} = V_{s11} = V_{s12} = 3V_{dc}. \quad (18)$$

where V_{Sn} represents peak voltage of switch when it is turn-off.

For this structure, the total standing voltage (TSV) is denoted as equation (19)

$$TSV = 4 * (V_{s1} + V_{s5} + V_{s9}) = 24V_{dc}. \quad (19)$$

The proportion of sum of switch turn-off voltages to peak voltage seems through the load is TSV $(p.u.)$. It is $4p.u.$ in present state for the proposed topology. Figure5 portrays a bar chart demonstrating voltage stress of individual switching device. At this instance for 13-level configuration TSV $(p.u.)$ is 4. Considering identical approach for 15-level configuration voltage stress and TSV are calculated. TSV $(p.u.)$ is identical to 13-level for 15-level configuration. For 13-level configuration blocking voltage of switches depicted as bar chart shown in Figure 5(a). From Figure 5(a), at $+6V_{dc}$ level S_1, S_2, S_5, S_6, S_9 and S_{10} switches are conducting and remaining switches are appeared as a nonconductive element. As a result, the blocking voltage of switches S_3 and S_4 is $1V_{dc}$, S_7 and S_8 are $2V_{dc}$, and S_{11} and S_{12} is $3V_{dc}$, respectively. Figure 5(a) depicts the blocking voltage of switches for a 13-level configuration in the same way that it does for other modes of operation. In similar fashion for 15-level configuration depicted in Figure 5(b).

3.3. Loss Analysis

Switching and conduction losses are different types of power losses experienced by switching devices. Conduction losses are brought on by on-state resistance

$$THD = \frac{\sqrt{\left(\left(\frac{\pi^2 p^2}{8}\right) - \left(\frac{\pi}{4}\left(\sum_{i=0}^{p-1}(2i-1)\,\alpha_i\right)\right) - \left(\sum_{i=1}^{p}\cos\alpha_i\right)^2\right)}}{\left(\sum_{i=1}^{p}\cos\alpha_i\right)}, \tag{13}$$

$$2^{nd}term = \frac{\pi}{4}(\alpha_1 + 3\alpha_2 + 5\alpha_3 + 7\alpha_4 + 9\alpha_5 + 11\alpha_6), \tag{14}$$

$$3^{rd}term = \cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 + \cos\alpha_5 + \cos\alpha_6. \tag{15}$$

while switching losses are a result of delays in the switch's on/off processes. It is possible to express the switching loss during the turn-on process as

$$P_{swlturnon}(i) = f_{carrier}\int_0^{t_{on}} v(t)i(t)dt$$
$$= f_{carrier}\int_0^{t_{on}} \left(\left(\frac{V_{swoff,i}}{t_{on}}(t_{on}-t)\right)\left(\frac{i_{on,i}}{t_{on}}t\right)\right)dt$$
$$= \frac{1}{6}f_{carrier} * V_{swoff,i} * i_{on,i} * t_{on}, \tag{20}$$

$$P_{swlturnoff}(i) = f_{carrier}\int_0^{t_{off}} v(t)i(t)dt$$
$$= f_{carrier}\int_0^{t_{off}} \left(\left(\frac{V_{swoff,i}}{t_{off}}t\right)\left(\frac{i_{off,i}}{t_{off}}(t_{off}-t)\right)\right)dt$$
$$= \frac{1}{6}f_{carrier} * V_{swoff,i} * i_{off,i} * t_{off}. \tag{21}$$

where $P_{swlturnon}(i)$, $P_{swltunoff}(i)$ and V_{swoff} denotes the ith switch's turn on, turn off loss, and off-state switching voltage, respectively. Currents during the switch's on- and off-states, respectively, are called I_{on} and I_{off}. Total switching losses (P_{sw}) are calculated by summing turn-on and turn-off losses.

$$P_{sw}(Total) = \sum_{i=1}^{N_{sw}}\left(\begin{array}{l}\sum_{j=1}^{N_{on}(i)} P_{swlon}\,(ij) \\ +\sum_{j=1}^{N_{off}(i)} P_{swloff}\,(ij)\end{array}\right) \tag{22}$$

where N_sw is the total number of switches of the proposed MLI.

Conduction losses are appeared in a switch during the conduction period due to on-state resistance and voltage drop across the switch. Generalized equation for conduction losses of diode and switch as follows

$$P_{Dcon} = V_{Don} * i_{Davg} + R_{Don} * i^2_{Drms} \tag{23}$$
$$P_{swcon} = V_{swon} * i_{swavg} + R_{swon} * i^2_{swrms}, \tag{24}$$

where P_{Dcon} and P_{swcon} are diode and switch conduction losses, V_{Don} and V_{swon} are on-state voltage drop of diode and switch respectively. R_{Don} and R_{swon} are on-state resistances of diode and switch, i_{Davg}, i_{swavg}, i_{Drms} and i_{swrms} are average and RMS currents of switch respectively.

4. Results & Discussion

4.1. Simulation Results

All the suggested configurations in the simulation are developed and simulated in an open-loop architecture employing the simulation tool MATLAB/Simulink. In the beginning, the switching angles of all techniques is determined related to first quadrant, and then the associated angles for the remaining quadrants estimated utilising quarter-wave symmetry estimations. Subsequently acquiring all switching angles for each cycle using the respective method, the corresponding switching time for each of the switching angles during that period is calculated numerically. At this instance, for 13-level configuration entirely 24 switching angles must be computed implying that 24 switching times accumulate using aforementioned methods for a cycle duration 50Hz. The switching modes as well as time have been implemented to operate in a manner if there is a absence of gate pulse, it represents as null output that corresponds to zero switching. Topology and modulation make sure zero switching at the beginning and intermediate points concerning positive cycle as well as negative cycle.

A standard grid filter is intended for ensuring the feasibility of the suggested asymmetrical configurations for integration into the grid since the resultant voltage is stepped wave thereby rendering it pure sinusoidal when the system is of open loop. This approach is additionally employed for further research with RL loads in order to make sure the reliability of the suggested inverters. In simple terms, an ordinary low pass passive T/π filter is built iteratively for frequency of 50 Hz considering equation (25)

$$f = \frac{1}{\pi\sqrt{LC}}. \tag{25}$$

It ought to be pointed out that distinct THD values related to various modulation index (MI) for all the methods addressed here are capable of being accomplished through modification of dc voltages solely since the switching angles remain unchanged for every

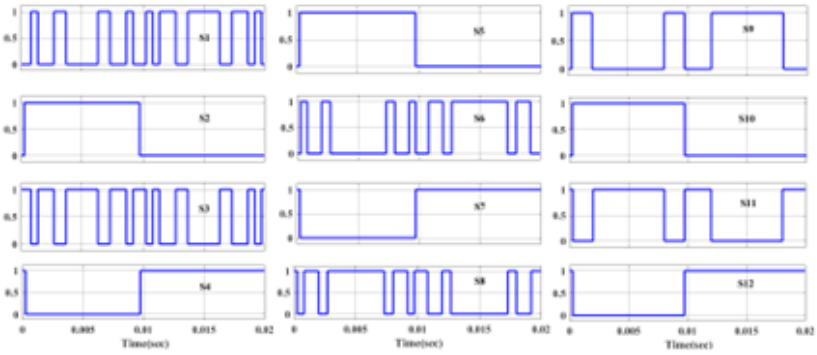


Fig. 6: Switching pulses for 13-level configuration

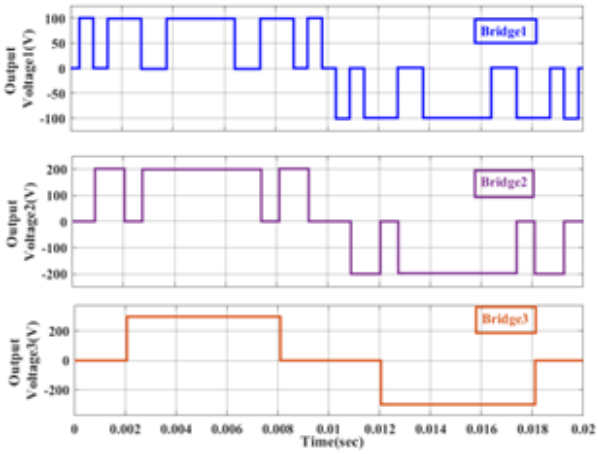


Fig. 7: Outputs of each bridge for HHM (13-level configuration)

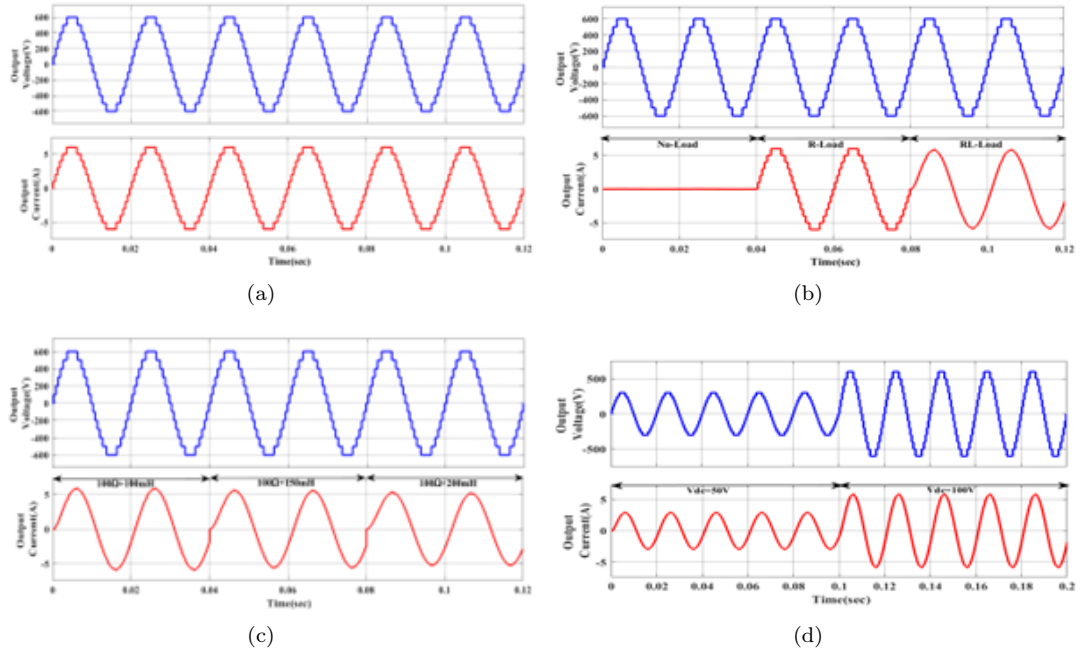
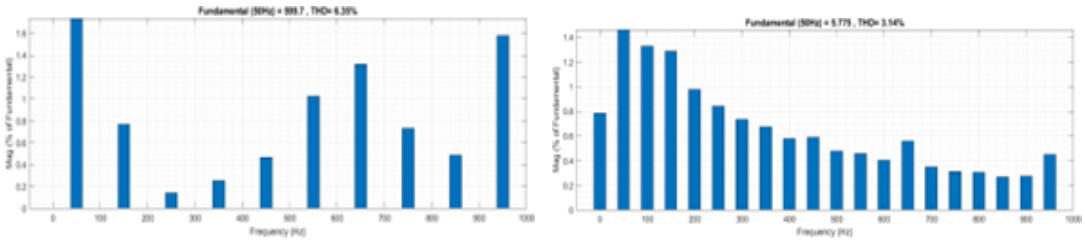


Fig. 8: Output Voltage and current for 13-level configuration with (a) R-load, (b) Various load scenarios, (c) Distinct RL-loads, (d) Change of source voltages.



(a) (b)

Fig. 9: %THD for 13-level configuration with (a) Output Voltage, (b) Output Current.

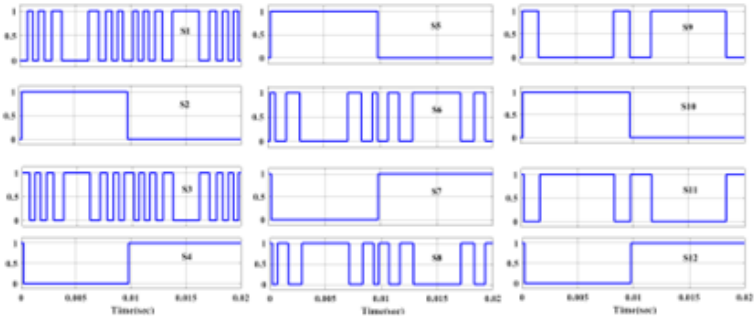


Fig. 10: switching pulses for 15-level configuration

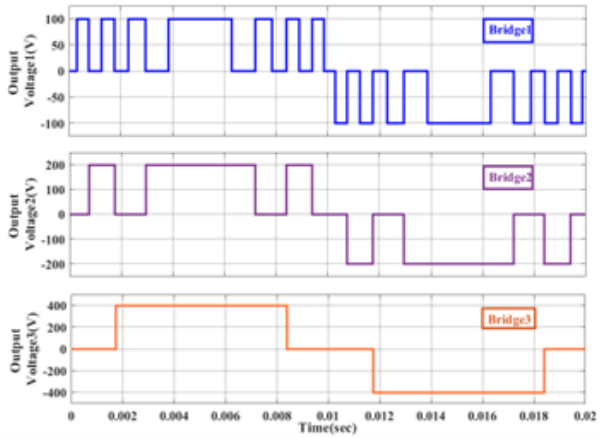


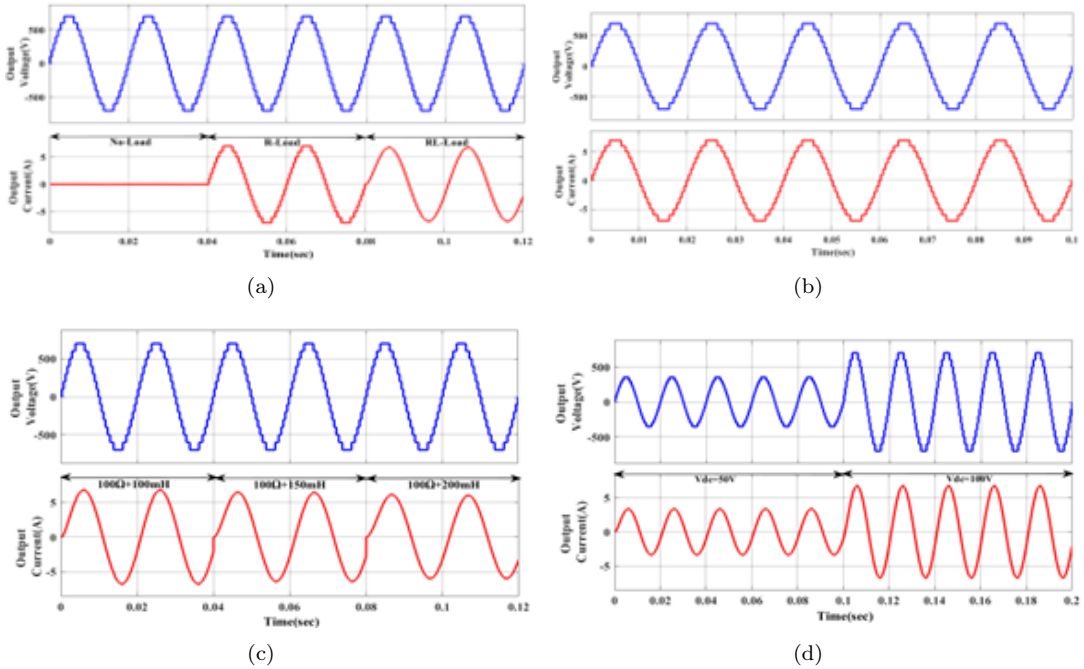
Fig. 11: Outputs of each bridge for HHM (15-level configuration)

technique. Respective MI for each method is additionally unique due to switching angle computations vary.

The NSCHBMLI technique is employed for creating the 13-level inverter in this case. For thirteen-level, source voltages are considered as 100V, 200V, and 300V respectively. At this instance, the load parameters are considered as 100Ω for resistance and 100mH for inductance. The proposed inverter's operating frequency is fundamental frequency or 50Hz. Figure 6 depicts the switching pulses created for a 13-level inverter configuration through HHM for a single cycle. Figure 7 represents all H bridge output for HHM, it shows that bridge1 peak output voltage is 100V, bridge2 maximum output voltage is 200V and bridge3 peak output voltage is 300V respectively.

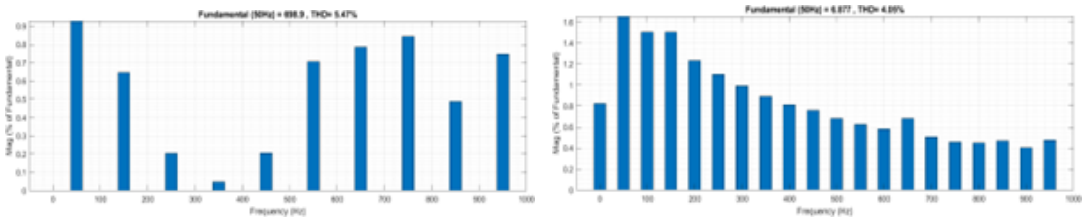
The functioning of the inverter according to R-load can be seen in Figure 8(a). The output current seems to be correlated to the output voltage. Figure 8(b) represents the inverter's outcomes for eleven-level operation depending on various load situations. Figure 8(b) indicates that output voltage remains constant regardless of loading conditions, but current is null during unloading, implying voltage for Resistive loads and delays for inductive loads. Figure 8(c) depicts variations of waveforms related to inductive load fluctuations. Figure 8(c) shows that as inductance increases, the current falls due to high inductive load leads more lagging of current. Figure 8(d) shows the performance of output voltage and current for variation in source voltages. Due to RL-Load whatever the variation of source voltage output current follows output voltage with lagging nature. Figure 9 shows the voltage and current harmonic spectrum including THD values for RL load. The %THD value for output voltage and current considering load as RL are 6.35 and 4.38 respectively.

The BCHBMLI technique is implemented to build the 15-level inverter. Source voltages for fifteen levels are 100V, 200V and 400V respectively. The load parameters are 100Ω for resistance and 100mH for inductance in this case. The operating frequency of the proposed inverter is 50Hz. Likewise, for Fifteen-level topology various loading conditions are considered for validating the inverter output performance. Figure



(a) (b) (c) (d)

Fig. 12: Output Voltage and current for 15-level configuration with (a) R-load, (b) Various load scenarios, (c) Distinct RL-loads, (d) Change of source voltages.



(a) (b)

Fig. 13: %THD for 15-level configuration with (a) Output Voltage, (b) Output Current.

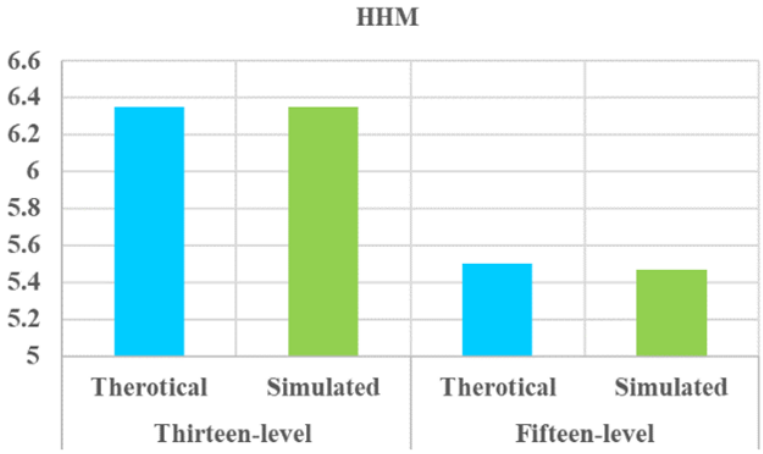


Fig. 14: Comparison of THD (%) for HHM

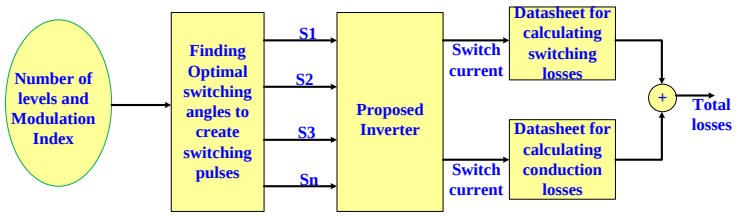
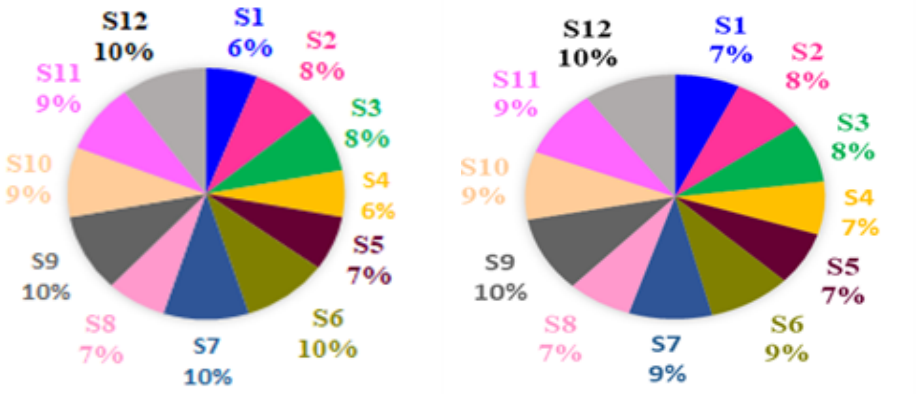
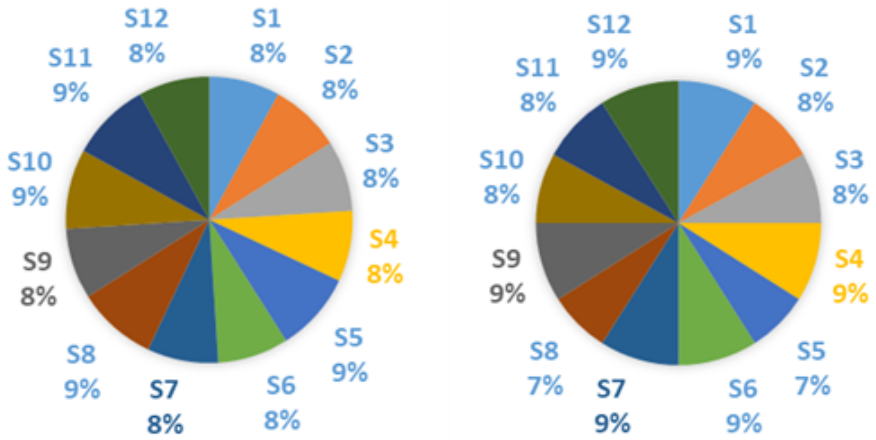


Fig. 15: Switching Loss analysis using PLECS Software



(a) (b)

Fig. 16: Percentage Losses of Thirteen -Level Inverter with (a) For R-Load, (b) For RL-Load.



(a) (b)

Fig. 17: Percentage Losses of Fifteen -Level Inverter with (a) For R-Load, (b) For RL-Load.

10 shows the switching pulses produced for 15-level inverter configuration during a single cycle through HHM. Figure 11 depicts all H bridge output for HHM, demonstrating that bridge1 peak output voltage is 100V, bridge2 peak output voltage is 200V, and bridge3 peak output voltage is 400V, respectively. Figure 12(a) shows the performance of the inverter under resistive loading condition. From Figure 12(a), current follows output voltage. Figure 12(b) indicates the operation of the inverter under various loading conditions. From Figure 12(b), it seems to be there is no variation of output voltage whatever the circumstances, only current effects based on loading. if there is no load current does not flow, if it is resistive current follows voltage, if it is sum of resistive and inductive then current becomes lagging with respect to voltage. Figure 12(c) illustrates the operating condition of inverter under different inductive loading conditions. From the observation of Figure 12(c), current reduces as load increases and becomes lagging in nature.

Figure 12(d) portrays the output voltage and current performance as source voltages vary. For the reason of RL-Load, regardless of the variation of source voltage, output current lags behind output voltage. Figure 13 depicts the voltage and current harmonic spectrum with THD values for an RL load.

The %THD values for output voltage and current are 5.47 and 4.05, respectively, when the load is RL. Figure 13 shows that there are very few low order harmonics with regard to the fundamental component. %THD values for other harmonic mitigation methods determined through simulation using the same procedure. Figure 14 depicts the THD comparison of HHM approach theoretical and simualted results are presented. In similar fashion for other methods simulation is performed. As a result, in comparison to other methods, the HHM approach is the best optimized harmonic mitigation technique.

4.2. Thermal Modelling

PLECS software serves to thermally model the power semiconductor devices of the suggested configuration. Figure 15 represents Loss analysis method carried out in PLECS Software.Figure 16(a) and 16(b) indicate the percentage of losses for semiconductor devices for thirteen-level operation at loading condition of 100Ω and 100Ω +100mH respectively. The efficiency is computed through simply R loads and displayed in favor of the output power (0-5000W). Similarly, Figures 17(a) and 17(b) indicate the percentage of losses for fifteen-level operation under the previously specified loading conditions. As shown in Figure 18, the effectiveness spans 98.2% to 97.0%. The efficiency declines as the load grows. Since when load rises, conduction losses

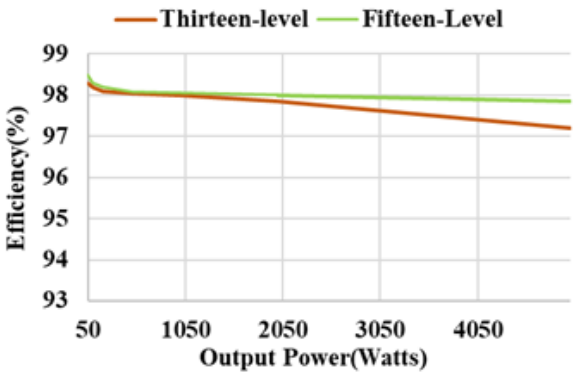


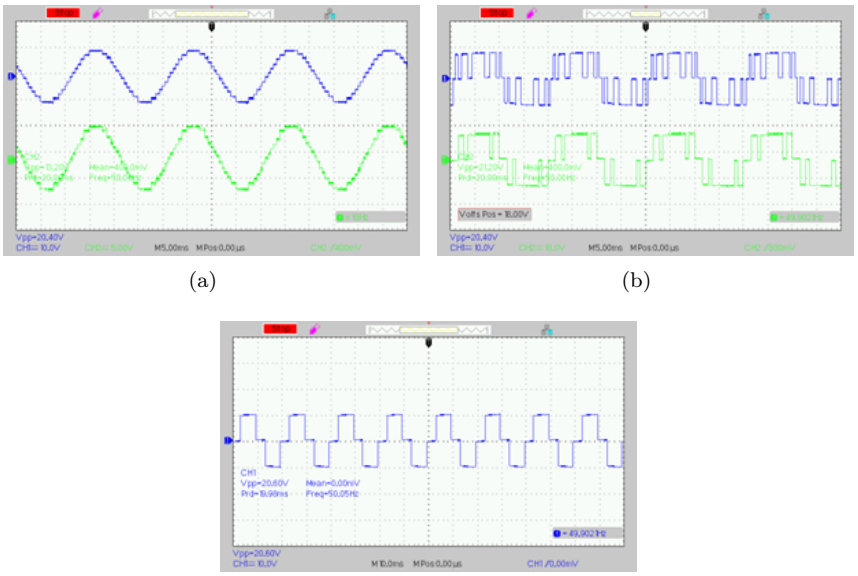
Fig. 18: Switching Loss analysis using PLECS Software

grow, which causes temperatures to rise, causing a decline in efficiency.

4.3. HIL Implementation

Real-time simulator plays a crucial role for designing and validating system effectiveness and accuracy since models built in real-time operate at an identical pace as real systems in existence. The OPAL-RT simulator links with the Sim Power System in MATLAB/Simulink employing the RT-LAB software. The OPAL-RT RT-LAB and eFPGAsim real-time platforms, along with advanced Intel processors and FPGA chips, are all bundled in the OP4510. This multi-rate FPGA-based architecture facilitates users to model power converters for HIL applications with a few time steps of less than 7 μs for INTEL CPU-based sections with a duration of fewer nanoseconds on the FPGA chip. Following that, an advanced PWM controller can regulate real hardware for Quick Control Modelling (QCM) services concerning timing improvement superior to 20 nanoseconds. The OP4510 can additionally be served as an independent semiconductor device test system with established models

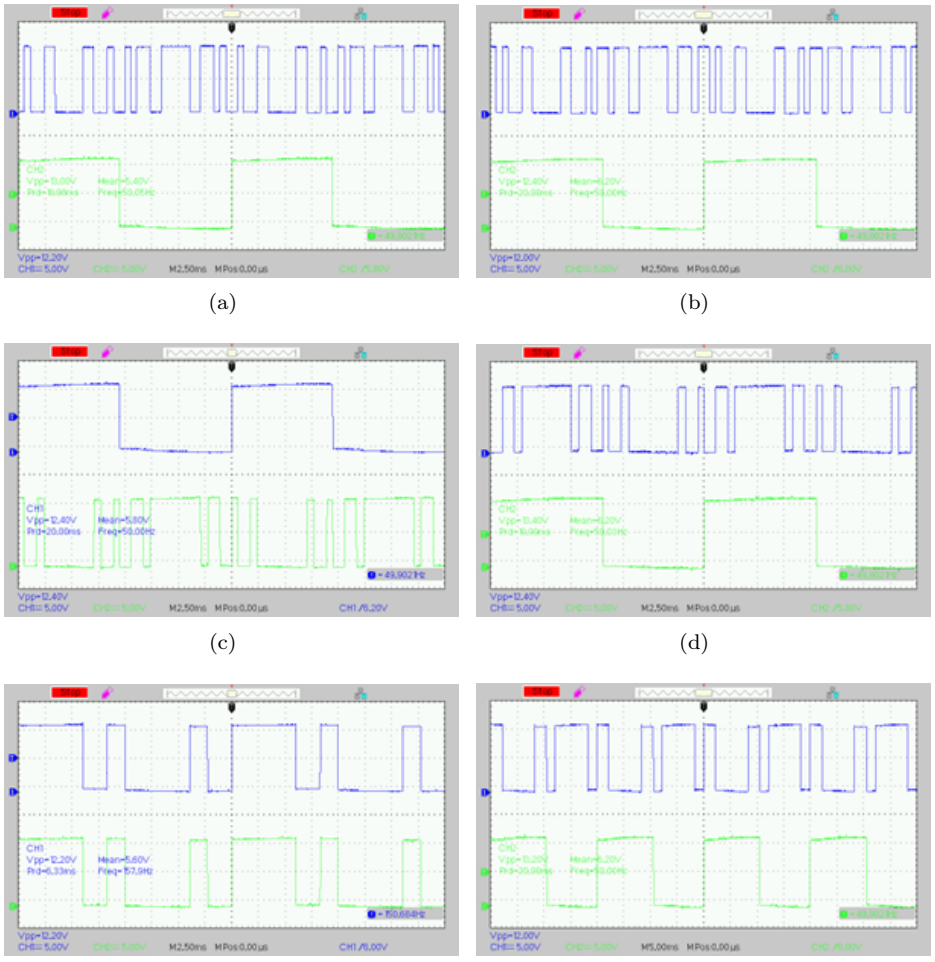
For HHM approach, the simulated waveforms of 13-level and 15-level are investigated through OPAL-RT(OP4510) environment are illustrated in Figures 19 to 22 respectively. Figure 19(a) indicates current follows voltage wave for R-Load. Figure 19(b)&19(c) shows voltage across three bridges for thirteen-level operation. It shows that OPAL-RT results and simualted results are in same fashion. The switching pulses of Thirteen-level for HHM is depicted in Figure 20. Likewise, for Fifteen-level real-time results are indicated in Figures 21-22 respectively. Figure 21(a) indicates Current is in correlation voltage for R-Load. Figures 21(b)&21(c) represents voltage across three bridges.The switching pulses are shown in Figure 22. For both Levels, HHM results are indicated as best results in contrast to other methods.



(a) (b)

(c)

Fig. 19: (a) Output Voltage and Current, (b)&(c) Voltage across bridges for Thirteen-Level Inverter.

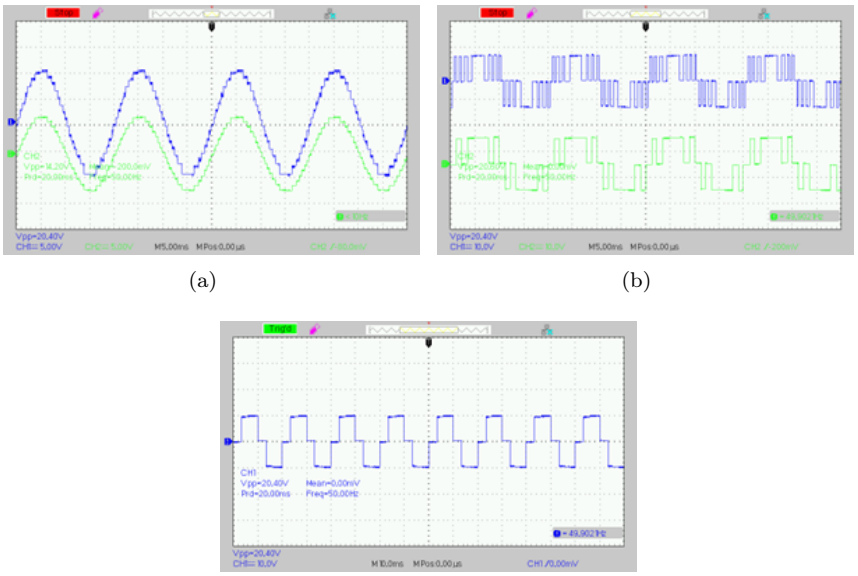


(a) (b)

(c) (d)

(e) (f)

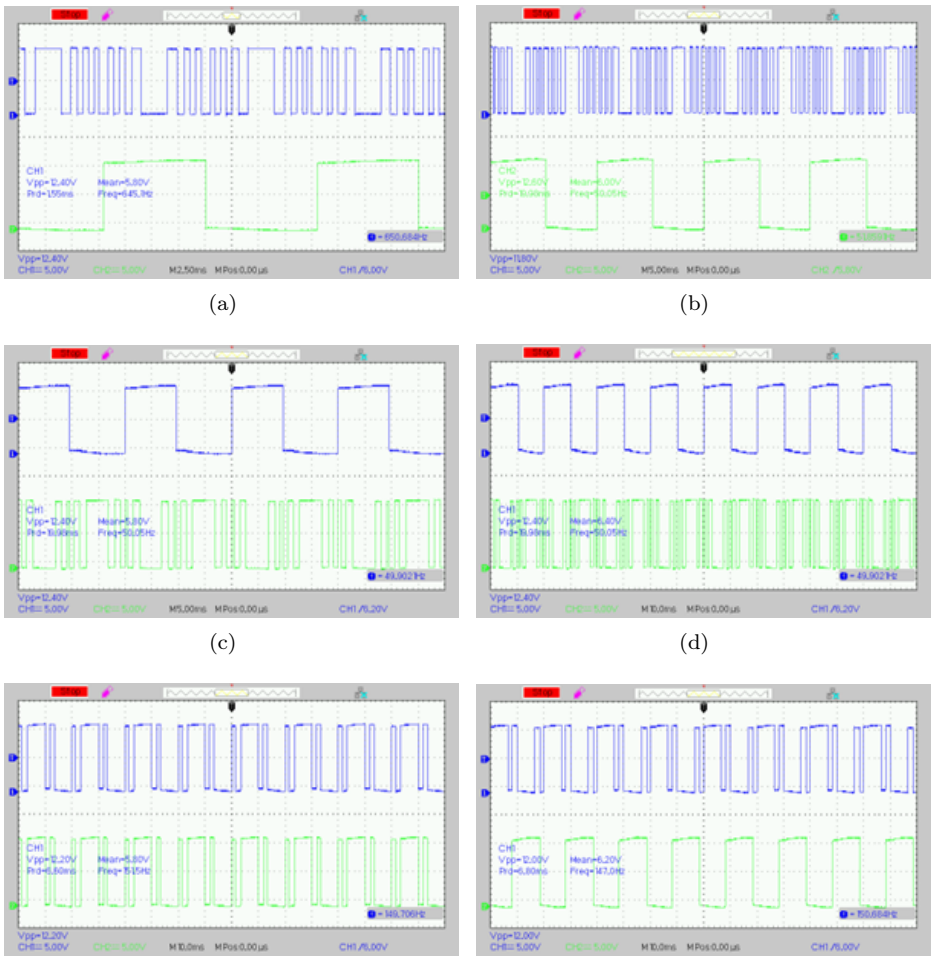
Fig. 20: Switching Pulses Of HHM for Thirteen-Level with (a) $(S_1 - S_2)$, (b) $(S_3 - S_4)$ (c) $(S_5 - S_6)$ (d) $(S_7 - S_8)$ (e) $(S_9 - S_{10})$ (f) $(S_{11} - S_{12})$.



(a) (b)

(c)

Fig. 21: (a) Output Voltage and Current, (b)&(c) Voltage across bridges for Fifteen-Level Operation.



(a) (b)

(c) (d)

(e) (f)

Fig. 22: Switching Pulses Of HHM for Fifteen-Level with (a) $(S_1 - S_2)$, (b) $(S_3 - S_4)$ (c) $(S_5 - S_6)$ (d) $(S_7 - S_8)$ (e) $(S_9 - S_{10})$ (f) $(S_{11} - S_{12})$.

Tab. 6: Comparison of Distinct 13-level Configurations

Parameters	[28]	[29]	[30]	Proposed
N_{Levels}	13	13	13	13
N_{Sw}	15	16	12	12
TSV	6	5	6	4
H-Bridge	No	No	No	No
Modulation Scheme	NLC	NLC	NLC	HHM
Pswloss	Low	Low	Low	Low
THD	Medium	Medium	Medium	Low

Tab. 7: Comparison of Various 15-level Configurations

Parameters	[25]	[26]	[27]	Proposed
N_{Levels}	15	15	15	15
N_{Sw}	16	14	12	12
TSV	6	5.5	5	4
H-Bridge	No	No	No	No
Modulation Scheme	NLC	Hybrid	LSPWM	HHM
Pswloss	Low	Medium	High	Low
THD	Medium	Medium	High	Low

5. Comparison

In this section, distinct MLI configurations related to thirteen level and fifteen level are presented in Table 6 and Table 7 respectively. The configuration in [28] requires 15 switches and operating scheme is NLC. In [29], the switches count is 16 and in similar to [28] it also operates utilizing NLC scheme. In [30] switches count is in same fashion as proposed and operating scheme is NLC. In comparison to other methods HHM provides minimum switching loss as well as THD.

Coming into fifteen level configurations [26] working on hybrid methodology (combination of HF scheme and LF scheme) and count of switches is 14. The functioning of configuration [27] is related to HF scheme and switches count is 12. Due to HF scheme losses are more than LF scheme and it is also related to working application. [29] needs 16 switches and control methodology is NLC. In contrast to other configurations proposed asymmetric configuration provides optimized results.

6. Conclusion

The recommended Cascaded bridge inverter utilizing asymmetrical operation presents anchored switching devices along with all three dc sources to produce output voltage patterns employing thirteen and fifteen levels. The present study built a simple control as well as modulation approach employing a mathematical switching method. By using PLECS software total losses are measured. In addition, the suggested configuration has reduced conduction and switching losses for accomplishing unique criteria in terms of cost factors and effectiveness. Likewise, the modified module using each kind of uneven dc sources, the suggested cascaded bridge structure can be implemented for distinct levels. Furthermore, THD in the proposed inverter output is minimum, as IEEE 519-2014 specifications. For HHM, optimized switching angle computation have been achieved by using numerical and simulation analysis, along with in the HIL approach for all the configurations. In relation to other methods, the simulation outcomes demonstrate the fact that HHM encounters lowest THD. Moreover, HHM exhibits highest RMS with precise variations in maximum output voltage along with current. Generally, photovoltaic panels through appropriate control methods are capable of being incorporated with the proposed topology for showing execution of grid either in on or off issues via an effective layout.

Author Contributions

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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About Authors

Lakshmi PRASANNA (corresponding author) was born in Rajahmundry, India. She received her B.E. and M. Tech from Andhra University and VJTI in 2008 and 2010, respectively. Presently she is working as a Research Scholar at Andhra University, Visakhapatnam. Her research interest includes Multilevel inverters, Electric Drives and Electric Vehicles.

Jyothsna. T.R. was born in Visakhapatnam, India. She received her M. Tech and Ph.D. from Andhra University, Visakhapatnam in 1997 and 2012 respectively. Presently she is working as a Professor in the Department of Electrical Engineering, Andhra University, Visakhapatnam. Her research interest includes Double fed Induction Generator (DFIG), Optimization techniques, Multilevel inverters, Electric Drives and Electric Vehicles.